Radiation Hardness Assurance of Field Programmable Gate Arrays in LHC Experiments

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Introduction

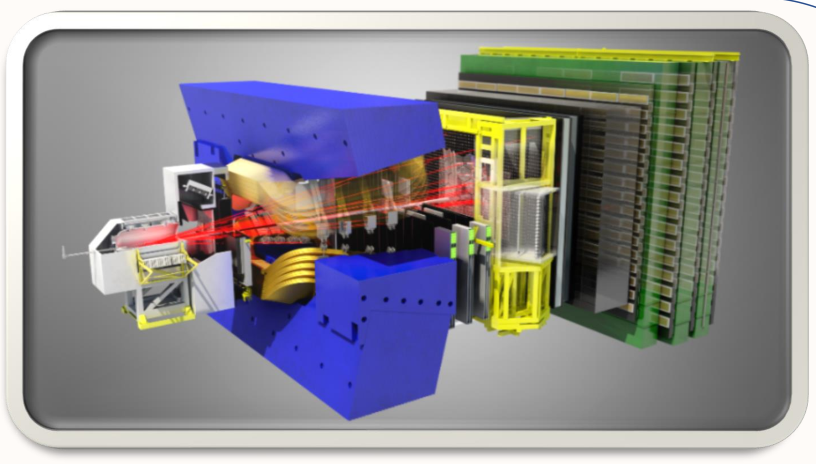
❖The commercial of the shelf components (COTS), especially FPGAs, have been considered for experiments in harsh environments with radiation background:
- ✓ Space experiments (e.g. ISS);
- ✓ Accelerator experiments (e.g. LHC at CERN);

❖The FPGAs are viable replacement solutions for Application Specific Integrated Circuits (ASICs) due to their:
- ✓ low cost;
- ✓ high logic density;
- ✓ low non-recurring engineering costs (NRE);

❖Though using FPGAs in such applications has several advantages, these devices are sensitive to radiation induced effects:
- ✓ Single Event Effects (SEEs);
- ✓ Cumulative effects (Total Ionizing Dose–TID and Displacement Damage–DD);

TID [krad]
200
Neutrons: 1 MeV n_{eq} [cm^{-2}]
$3 \cdot 10^{12}$
Hadrons: > 20 MeV [cm^{-2}]
$1.2 \cdot 10^{12}$

LHCb Upgraded RICH 1 Engineering Design Review Report



LHCb detector

❖During the second LHC long shutdown, started in 2019, the LHCb detector and its sub-detectors will be upgraded to operate at a higher luminosity;

LHCb Upgrade Phase I

❖SRAM-based FPGAs (KINTEX-7) were selected to be used in the digital readout boards of the LHCb RICH sub-detectors, for their sensors and frontend electronics;
- ✓ Microsemi's antifuse FPGAs are the backup solution;

❖An irradiation testing campaign has been implemented and established the radiation tolerance for both devices.

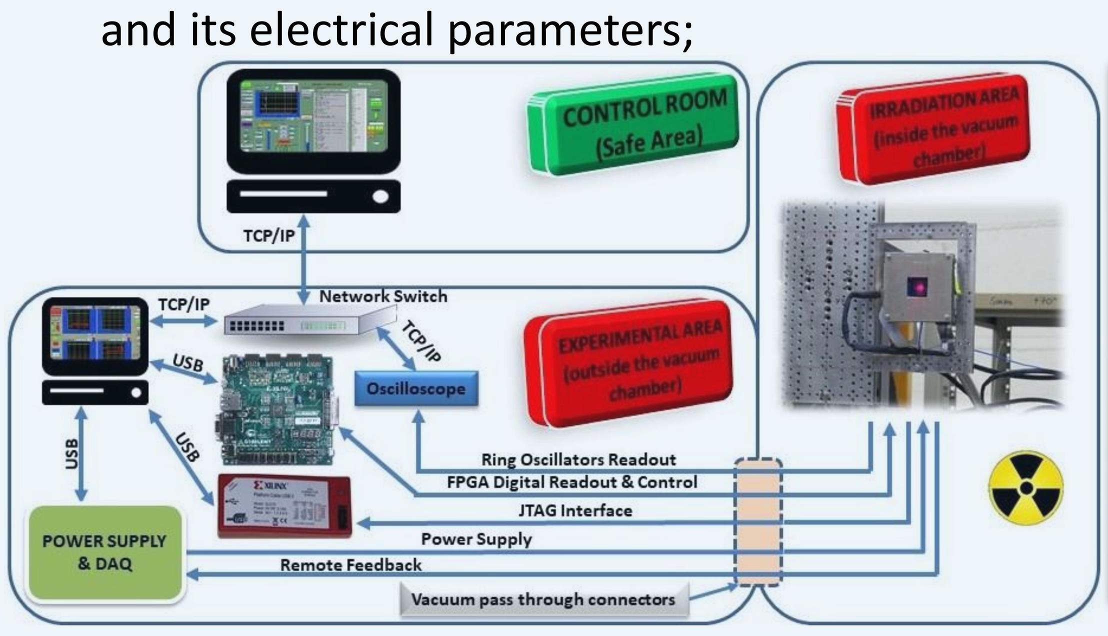
SRAM-Based FPGA

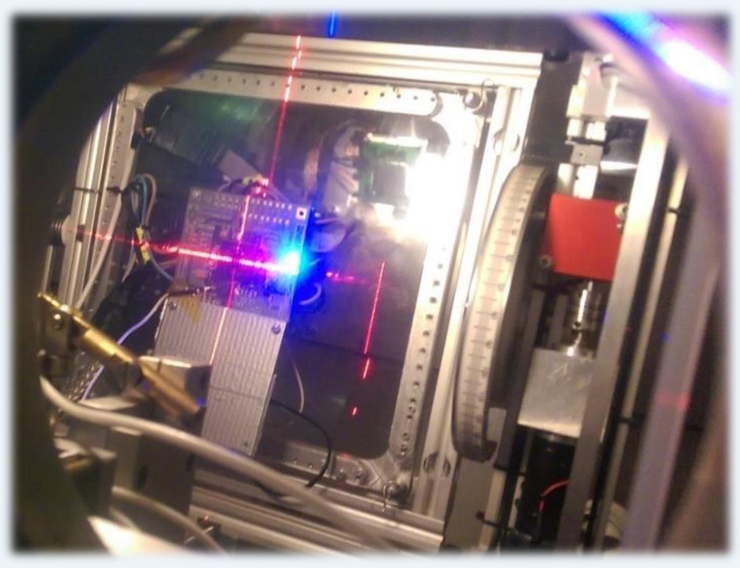
❖ The smallest device from Xilinx's KINTEX-7 family has been tested, **XC7K70T-FBG484C**:
- ✓ manufactured on 28 nm HKMG technology node based on TMSC's high performance and low power process (HPL);
- ✓ 82 k user Flip-Flops, 4.86 Mb of Block RAM (BRAM), 300 I/Os, 18.8 Mb of configuration memory (CRAM);

❖ Different particle beams were used to measure its radiation tolerance:
- ✓ 35 MeV and 200 MeV protons; (Juliech FZJ and PSI)
- ✓ Ions with a broad range of Linear Energy Transfer (LET): from 1.3 to 32.4 MeV · cm^2/mg; (Louvain CRC and Legnaro LNL)
- ✓ 8-50 KeV X-ray photons; (Padova University)
- ✓ Mixed field of particles from 24 GeV protons on a Copper target at CHARM CERN.

❖ Several resources were tested: CRAM, BRAM, user Flip-Flops (with TMR) and the IO Blocks;

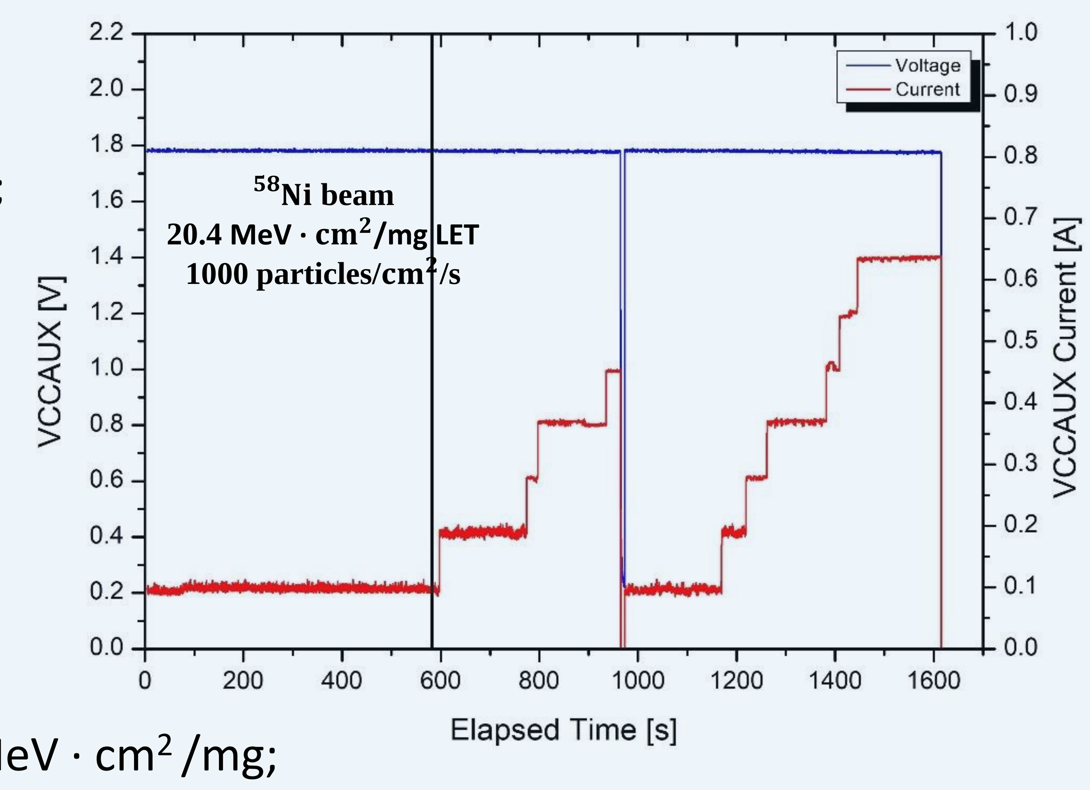
❖ A custom DAQ system has been designed to monitor the device firmware activity and its electrical parameters;





❖TID results

- ➢ 4 samples were tested with a TID from 0.44 up to 1 Mrad (Si);
- ➢ **35 MeV protons:**
- ✓ CRAM SEU cross-section: $4.9 \cdot 10^{-15}$ cm^2/bit;
- ✓ BRAM SEU cross-section: $6.9 \cdot 10^{-15}$ cm^2/bit;
- ✓ IO blocks SEU cross-section: $2.22 \cdot 10^{-11}$ cm^2/device.



❖Ion SEE results

- ✓ SEL LET threshold: around 15 MeV · cm^2/mg;
- ✓ SEFI events seen at LET of 32 MeV · cm^2/mg;
- ✓ CRAM SEU threshold: LET below 1.3 MeV · cm^2/mg;
- ✓ CRAM SEU cross-section at LET=1.3 MeV · cm^2/mg: $0.47 \cdot 10^{-10}$ cm^2/bit;
- ✓ CRAM SEU cross-section at 32 MeV · cm^2/mg LET: $0.26 \cdot 10^{-8}$ cm^2/bit;
- ✓ IO blocks SEU cross-section at LET of 8.59 MeV · cm^2/mg: $0.6 \cdot 10^{-5}$ cm^2/device;
- ✓ high current states were observed in the VCCINT (core) power rail (20 times larger than its baseline value), but recovered with full reconfiguration;
- ✓ micro-latchups highlighted by 100 mA current jumps in the VCCAUX power rail were seen, but recovered with power cycle.

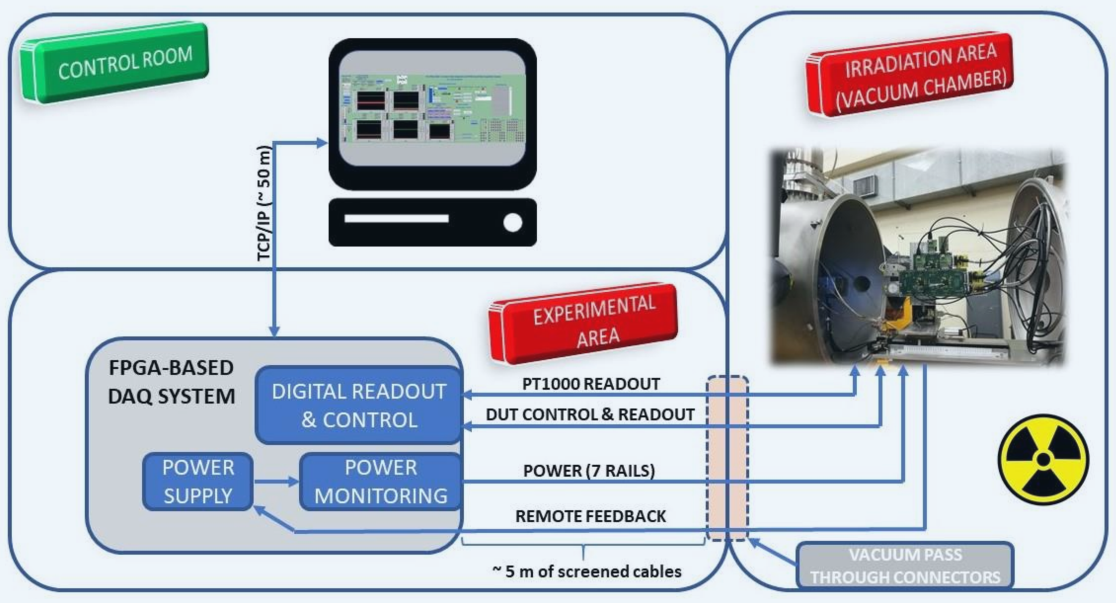
Antifuse FPGA

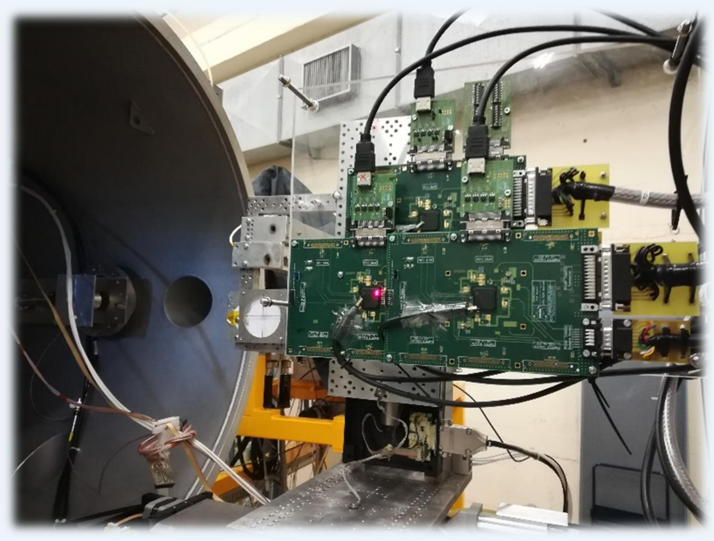
❖ An FPGA from Microsemi's Axcelerator family has been chosen, **AX250-FBG484**:
- ✓ 0.15 µm CMOS antifuse process technology, one time programmable;
- ✓ 1408 register cells (R-cells), 2816 combinational cells (C-cells), 55 kb of embedded RAM, 248 I/Os, 4 hardwired clocks and 4 routed clocks;

❖ So far, the FPGA was tested with 20 MeV protons at SIRAD facility from Legnaro, and with 8-50 KeV X-ray at University of Padova;

❖ Several versions of firmware were used in irradiation tests:
- ✓ R-cells with a TMR architecture and a minority voter (up to 60 %);
- ✓ R-cells, C-cells and I/O blocks configured to read 128 passive inputs;
- ✓ Embedded RAM test firmware (up to 70 %);

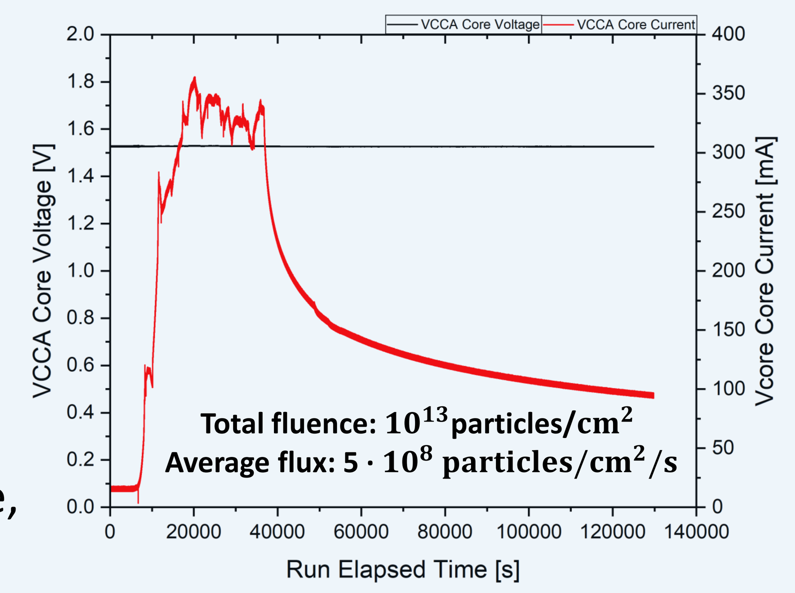
❖ Custom DAQ system designed to monitor the device and its firmware activity;





❖TID results:

- ✓ the FPGA prove to be resilient to high dose rates, 1 krad/s, and high TID, 8 Mrad (Si);
- ✓ the logic error rates were very low;
- ✓ the embedded RAM prove to be sensible to proton induced SEUs: $3.6 \cdot 10^{-14}$ cm^2/bit;
- ✓ high leakage current was seen in the core power rail at high TID with very high dose rate, over 0.3 Mrad (Si);
- ✓ the current variation is correlated with the high dose, and most fast changes due to beam fluctuations;
- ✓ proton induced TID effects were confirmed by X-Ray runs;
- ✓ annealing tests have been carried out after each irradiation test, and show a strong annealing effect in device over 1 h to 7 days.



Operation in the LHCb Environment

❖For the SRAM-based FPGA while operating in the Phase I of the LHCb Upgrade we expect ~ 20 – 30 k configuration SEUs per hour in about 1200 devices;
- ✓ Most of them will not affect the user logic, but a very small fraction can induce high current events which can disturb the FPGA operation or affects the information flow.

❖ The antifuse FPGA will not show any radiation induced effects if will be used during the Phase I of the LHCb Upgrade;
- ✓ However, its main drawback is the fact that is a one-time programmable device.

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